WHAT IS CLAIMED IS:

1. A method of conserving power consumption in a multi-processor data processing system, comprising:

monitoring a workload of the system;

determining a number of processors required to process the monitored workload at a predetermined performance criterion;

activating or deactivating processors to conform the number of active processors in the system to the determined number of processors; and

processing the workload with the active processors while maintaining the deactivated processors in a reduced power state.

2. The method of claim 1, wherein determining the number of processors required comprises determining the minimum number of processors required to achieve the performance criterion.

3. The method of claim 1, wherein deactivating a processor includes selecting a processor for deactivation based on the processor's workload.

4. The method of claim 1, wherein deactivating a processor includes migrating processes pending on a processor selected for deactivation to another processor.

5. The method of claim 4, wherein deactivating a processor further includes flushing the processor's cache memory before deactivating the processor.

6. The method of claim 1, wherein deactivating a processor comprises transitioning a processor to the lowest power state supported by the processor.

7. The method of claim 1, wherein monitoring the workload comprises determining the demand for CPU cycles.

8. The method of claim 7, wherein monitoring the workload includes determining the instantaneous workload periodically and averaging the instantaneous workload data to obtain an average workload.

9. A data processing system including processor, memory, and I/O means, the system including a sequence of processor executable instructions for conserving power, the instructions being stored on a computer readable medium, comprising:

computer code means for monitoring a workload of the system;

computer code means for determining a number of processors required to process the monitored workload at a predetermined performance criterion;

computer code means for activating or deactivating processors to conform the number of active processors in the system to the determined number of processors; and

computer code means for processing the workload with the active processors while maintaining the deactivated processors in a reduced power state.

10. The system of claim 9, wherein the code means for determining the number of processors required comprises code means for determining the minimum number of processors required to achieve the performance criterion.

11. The system of claim 9, wherein the code means for deactivating a processor includes code means for selecting a processor for deactivation based on the processor's workload.

12. The system of claim 9, wherein the code means for deactivating a processor includes code means for migrating processes pending on a processor selected for deactivation to another processor.

13. The system of claim 12, wherein the code means for deactivating a processor further includes code means for flushing the processor's cache memory before deactivating the processor.

14. The system of claim 9, wherein the code means for deactivating a processor comprises code means for transitioning a processor to the lowest power state supported by the processor.

15. The system of claim 9, wherein the code means for monitoring the workload comprises code means for determining the demand for CPU cycles.

16. The system of claim 15, wherein the code means for monitoring the workload includes code means for determining the instantaneous workload periodically and averaging the instantaneous workload data to obtain an average workload.

17. A computer program product comprising a sequence of processor executable instructions for conserving power, the instructions being stored on a computer readable medium, comprising:

computer code means for monitoring a workload of the system;

computer code means for determining a number of processors required to process the monitored workload at a predetermined performance criterion;

computer code means for activating or deactivating processors to conform the number of active processors in the system to the determined number of processors; and

computer code means for processing the workload with the active processors while maintaining the deactivated processors in a reduced power state.

18. The computer program product of claim 17, wherein the code means for determining the number of processors required comprises code means for determining the minimum number of processors required to achieve the performance criterion.

19. The computer program product of claim 17, wherein the code means for deactivating a processor includes code means for selecting a processor for deactivation based on the processor's workload.

20. The computer program product of claim 17, wherein the code means for deactivating a processor includes code means for migrating processes pending on a processor selected for deactivation to another processor.

21. The computer program product of claim 20, wherein the code means for deactivating a processor further includes code means for flushing the processor's cache memory before deactivating the processor.

22. The computer program product of claim 17, wherein the code means for deactivating a processor comprises code means for transitioning a processor to the lowest power state supported by the processor.

23. The computer program product of claim 17, wherein the code means for monitoring the workload comprises code means for determining the demand for CPU cycles.

24. The computer program product of claim 23, wherein the code means for monitoring the workload includes code means for determining the instantaneous workload periodically and averaging the instantaneous workload data to obtain an average workload.